FIG.1

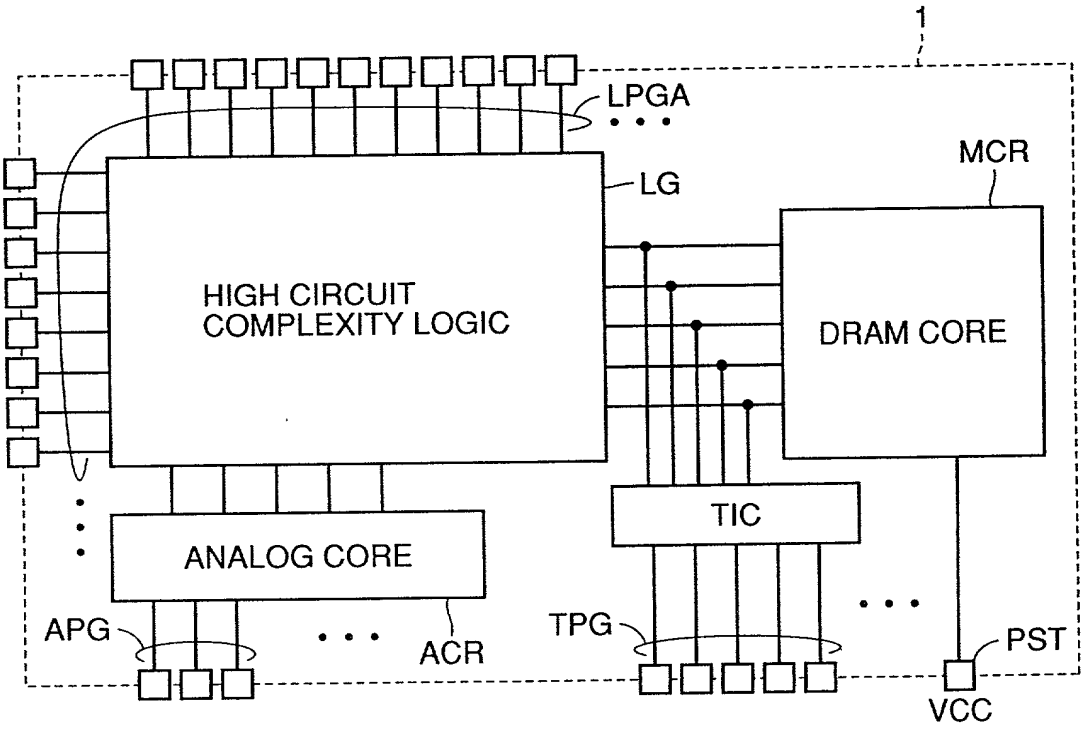
1
LPGA
MCR
LG
HIGH CIRCUIT
COMPLEXITY LOGIC
DRAM CORE
TIC
ANALOG CORE
APG
ACR
TPG
PST
VCC

FIG.2

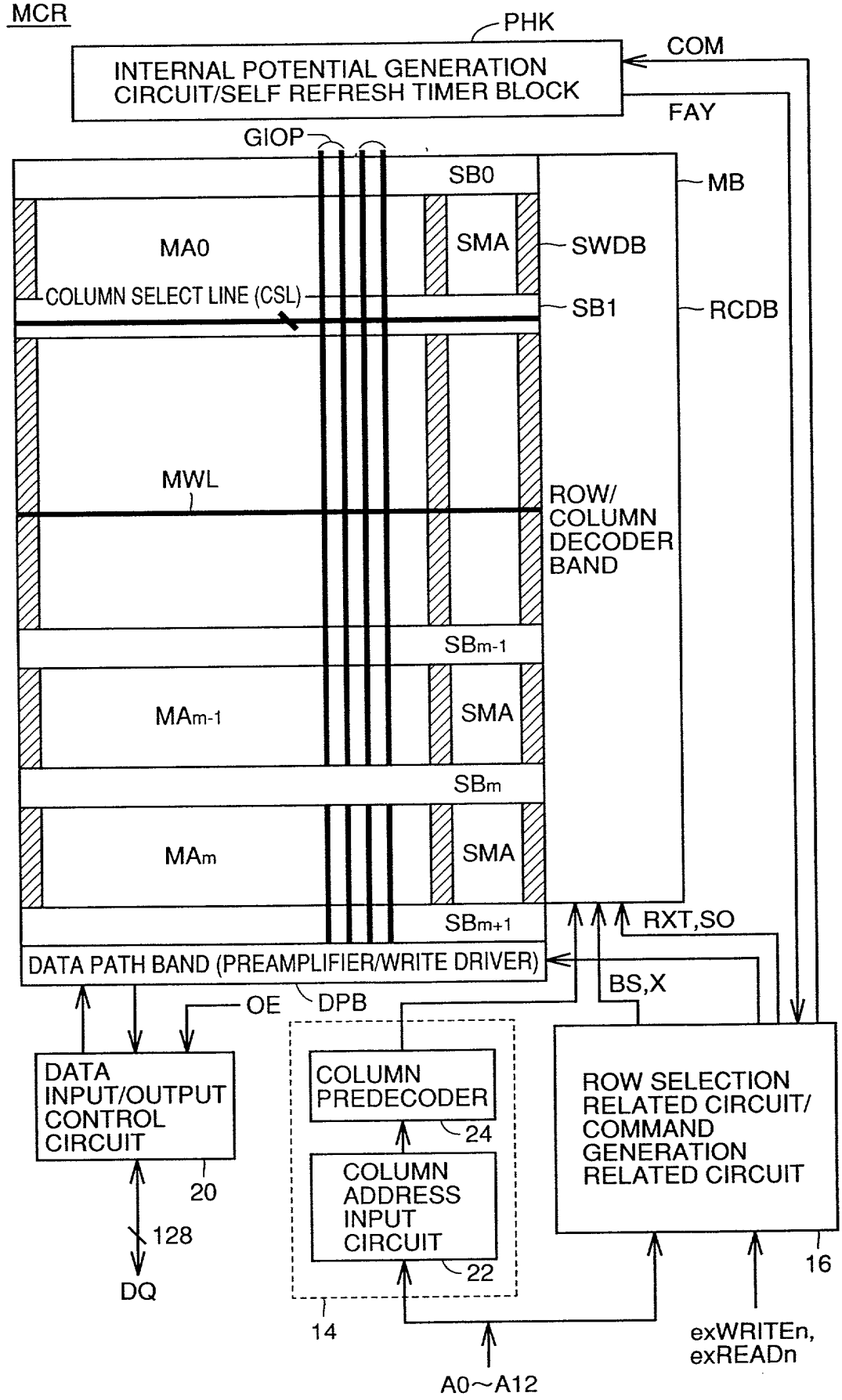
MCR
PHK
INTERNAL POTENTIAL GENERATION CIRCUIT/SELF REFRESH TIMER BLOCK
COM
FAY
GIOP
SB0
MB
MA0
SMA
SWDB
COLUMN SELECT LINE (CSL)
SB1
RCDB
MWL
ROW/ COLUMN DECODER BAND
SBm-1
MAm-1
SMA
SBm
MAm
SMA
SBm+1
RXT,SO
DATA PATH BAND (PREAMPLIFIER/WRITE DRIVER)
BS,X
OE
DPB
DATA INPUT/OUTPUT CONTROL CIRCUIT
20
128
DQ
COLUMN PREDECODER
24
COLUMN ADDRESS INPUT CIRCUIT
22
14
ROW SELECTION RELATED CIRCUIT/ COMMAND GENERATION RELATED CIRCUIT
16
exWRITEn, exREADn
A0~A12

FIG.3

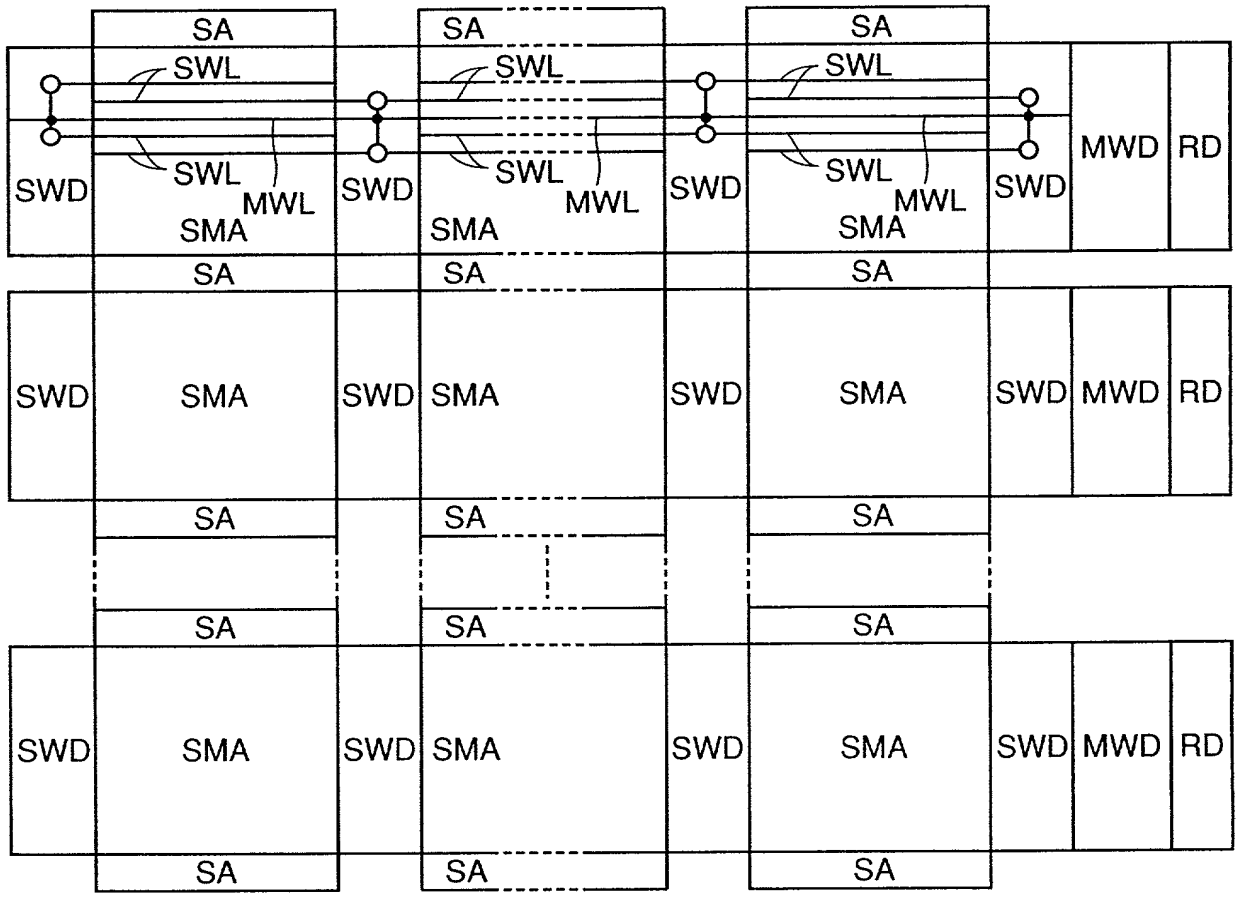

FIG.4

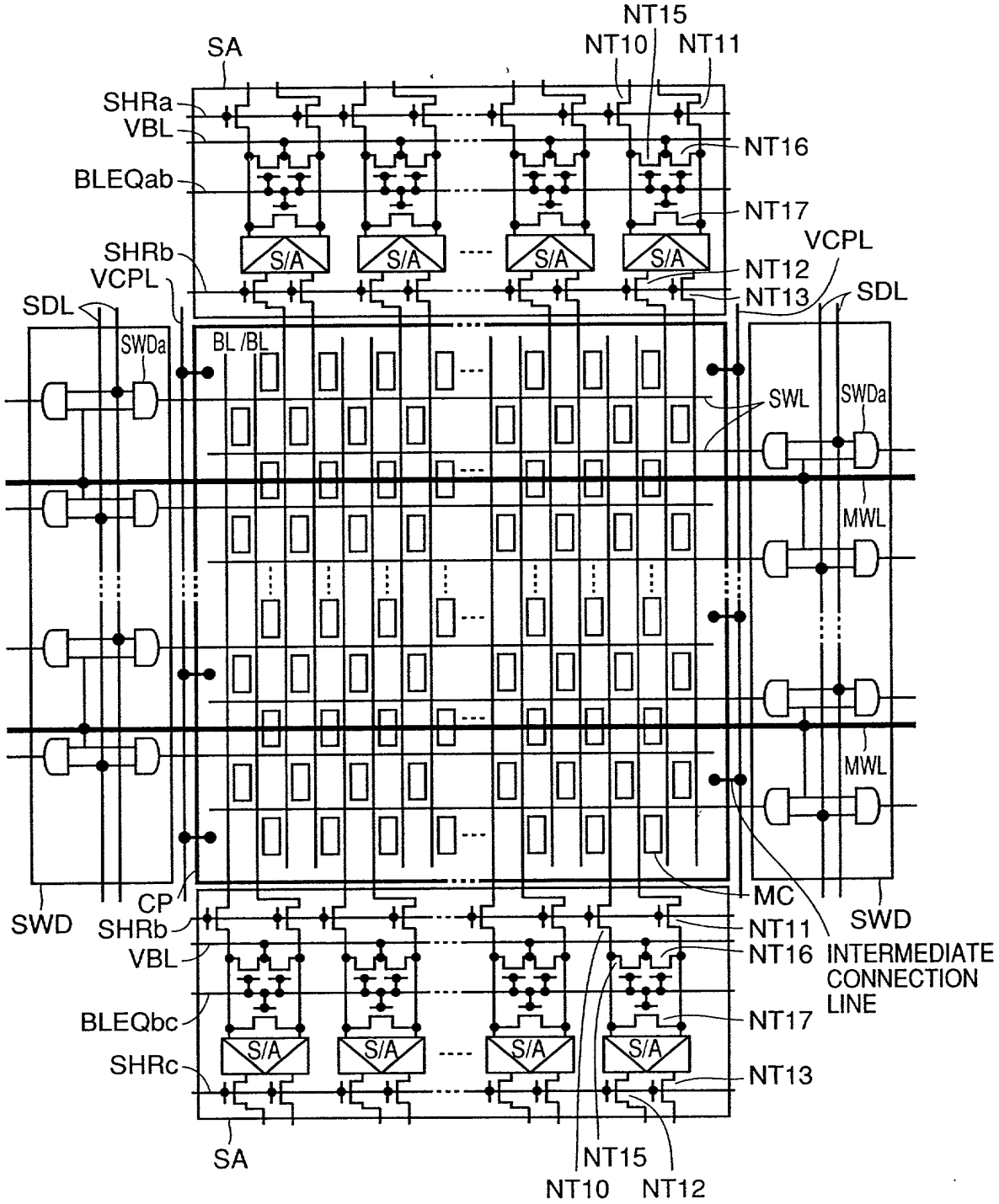
NT15
SA
NT10
NT11
SHRa
VBL
NT16
BLEQab
NT17
VCPL
SHRb
S/A
NT12
VCPL
NT13
SDL
SDL
SWDa
BL /BL
SWL
SWDa
MWL
MWL
MC
CP
SWD
SHRb
NT11
SWD
VBL
NT16
INTERMEDIATE CONNECTION LINE
BLEQbc
NT17
SHRc
NT13
SA
NT15
NT10
NT12

FIG.5

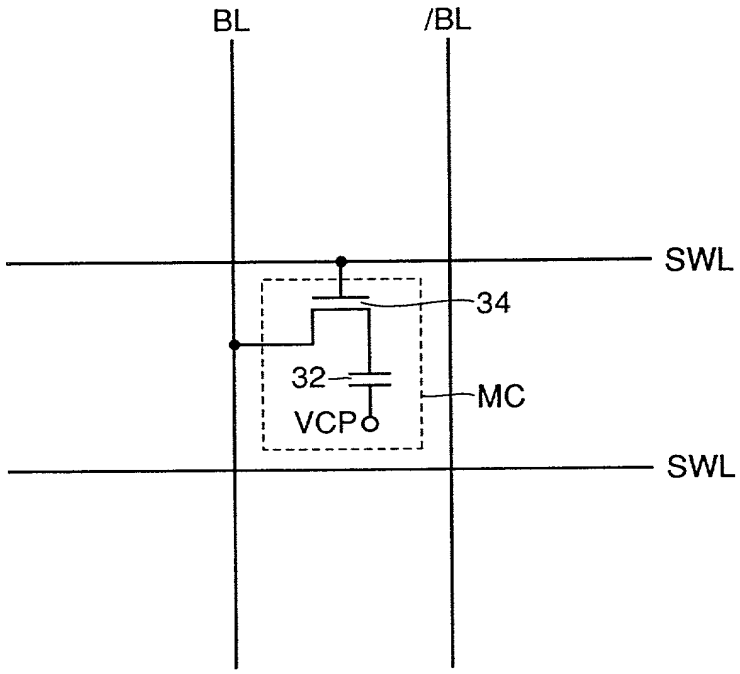

FIG.6

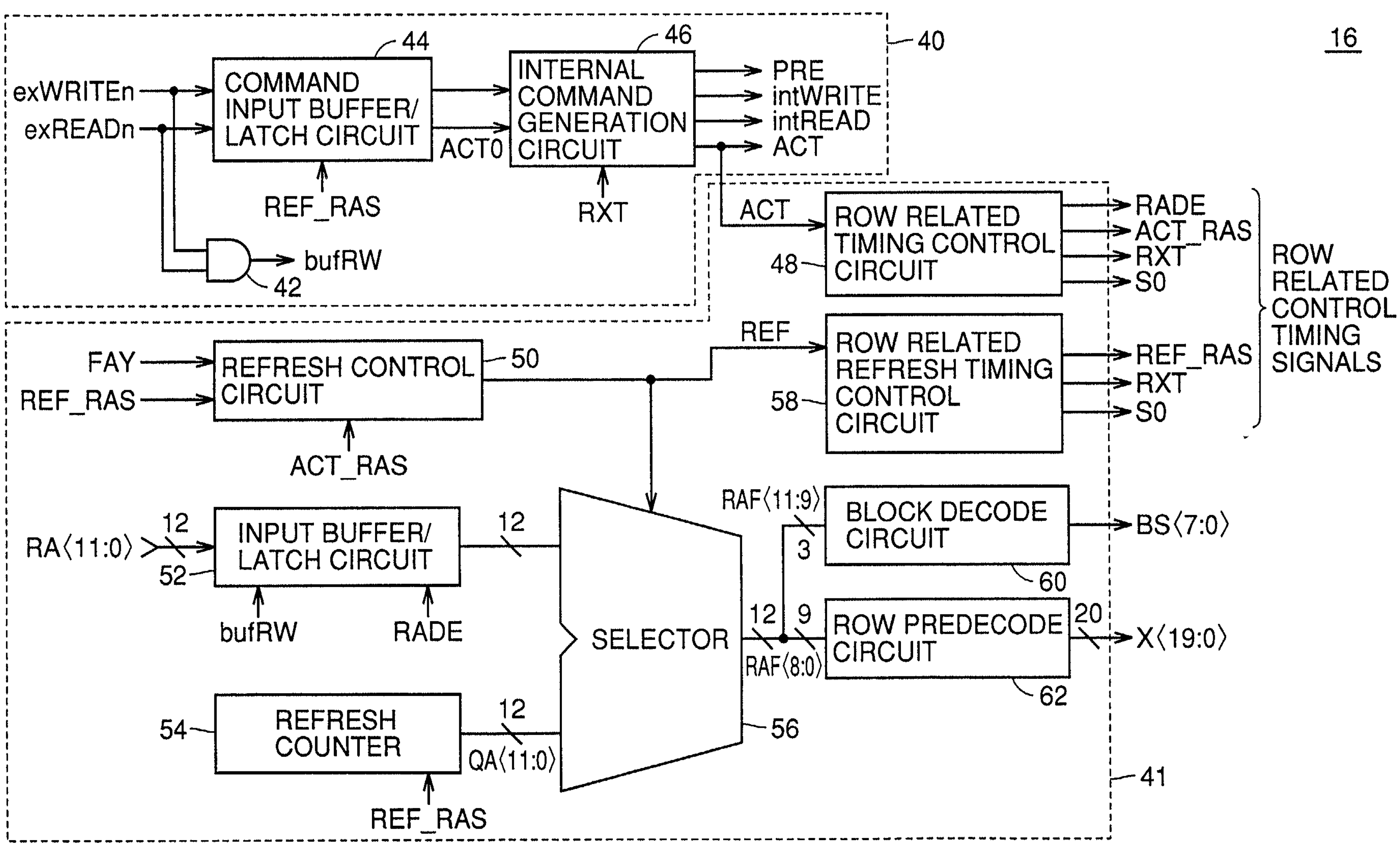
16
40
41
exWRITEn
exREADn
COMMAND INPUT BUFFER/ LATCH CIRCUIT
44
REF_RAS
ACT0
INTERNAL COMMAND GENERATION CIRCUIT
46
RXT
PRE
intWRITE
intREAD
ACT
bufRW
42
ACT
ROW RELATED TIMING CONTROL CIRCUIT
48
RADE
ACT_RAS
RXT
S0
ROW RELATED CONTROL TIMING SIGNALS
FAY
REF_RAS
REFRESH CONTROL CIRCUIT
50
ACT_RAS
REF
ROW RELATED REFRESH TIMING CONTROL CIRCUIT
58
REF_RAS
RXT
S0
RA〈11:0〉
12
52
INPUT BUFFER/ LATCH CIRCUIT
bufRW
RADE
12
SELECTOR
56
REFRESH COUNTER
54
REF_RAS
12
QA〈11:0〉
RAF〈11:9〉
3
BLOCK DECODE CIRCUIT
60
BS〈7:0〉
12
9
RAF〈8:0〉
ROW PREDECODE CIRCUIT
62
20
X〈19:0〉

FIG.7

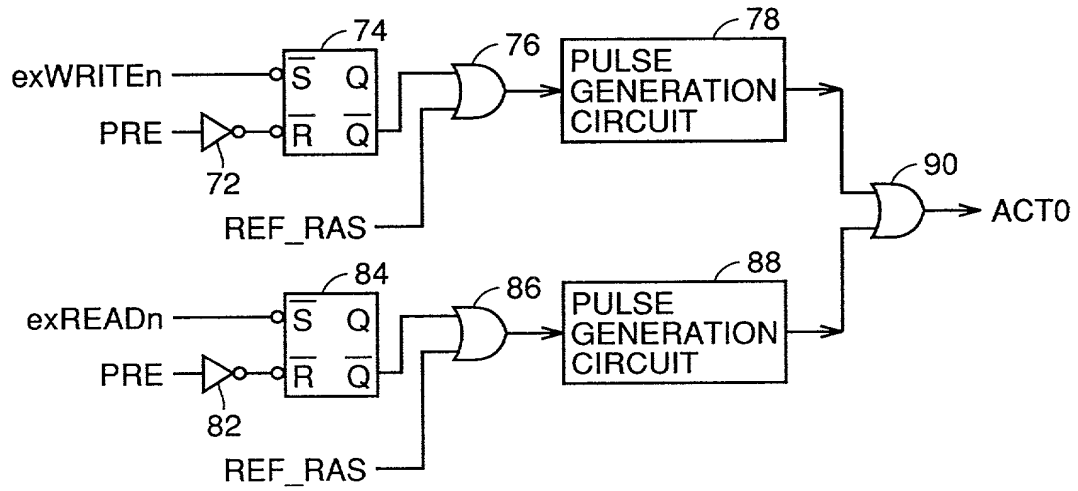
44
74
76
78
exWRITEn
PRE
S
Q
R
Q
72
REF_RAS
PULSE GENERATION CIRCUIT
90
ACT0
84
86
88
exREADn
PRE
S
Q
R
Q
82
REF_RAS
PULSE GENERATION CIRCUIT

FIG.8

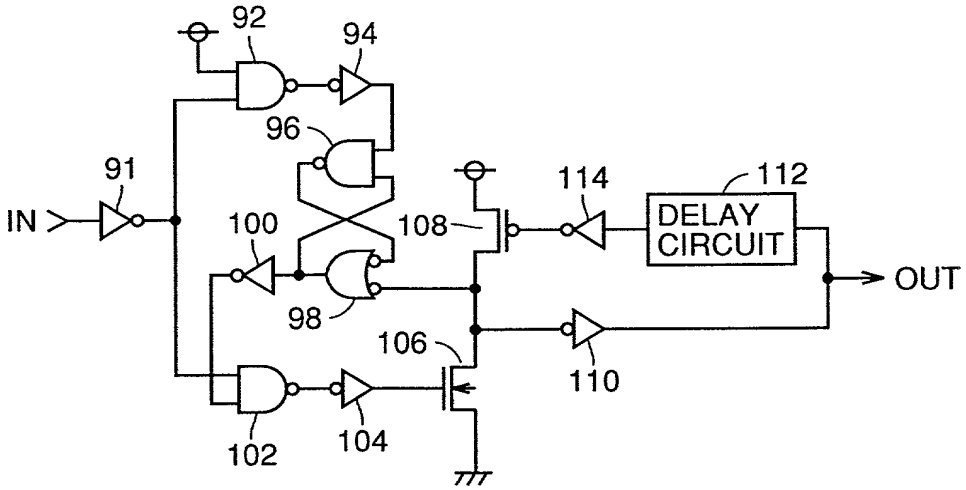
78
92
94
96
91
IN
100
108
114
112
DELAY CIRCUIT
OUT
98
106
110
102
104

FIG.9

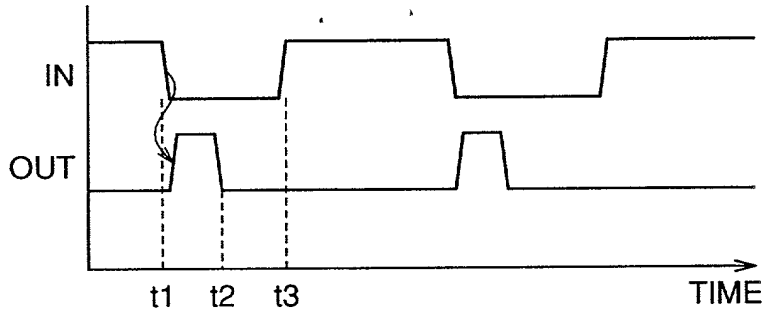

FIG.10

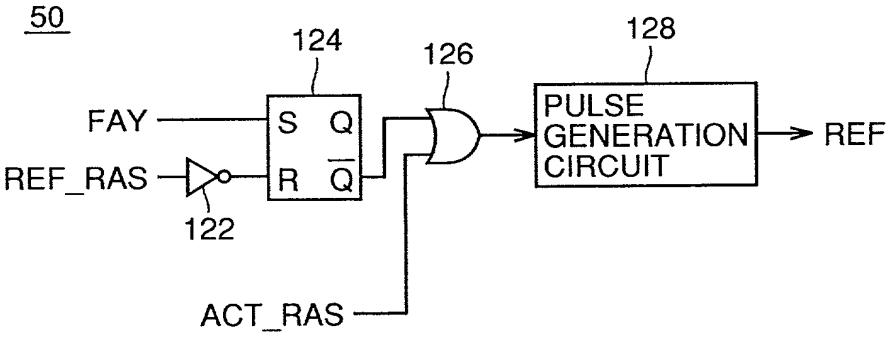

FIG.11

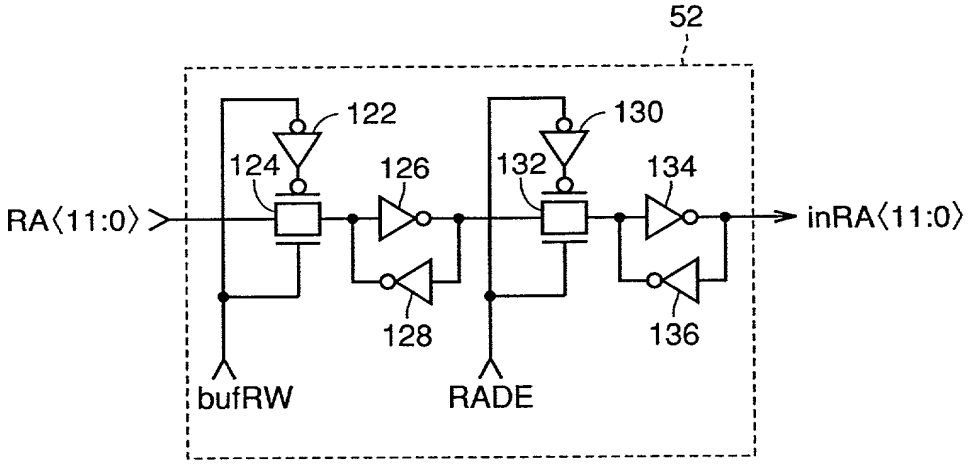

FIG. 12

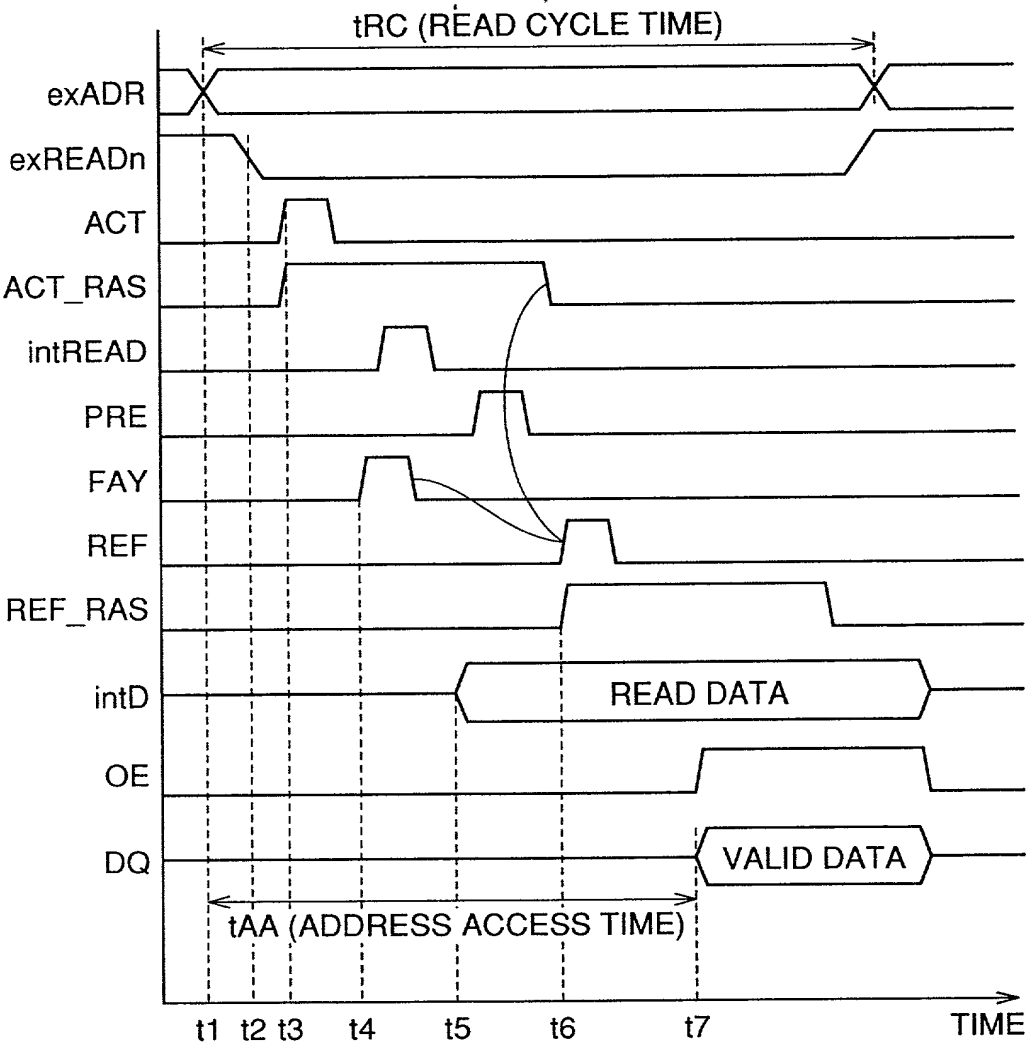
tRC (READ CYCLE TIME)
exADR
exREADn
ACT
ACT_RAS
intREAD
PRE
FAY
REF
REF_RAS
intD
READ DATA
OE
DQ
VALID DATA
tAA (ADDRESS ACCESS TIME)
t1
t2
t3
t4
t5
t6
t7
TIME

FIG.13

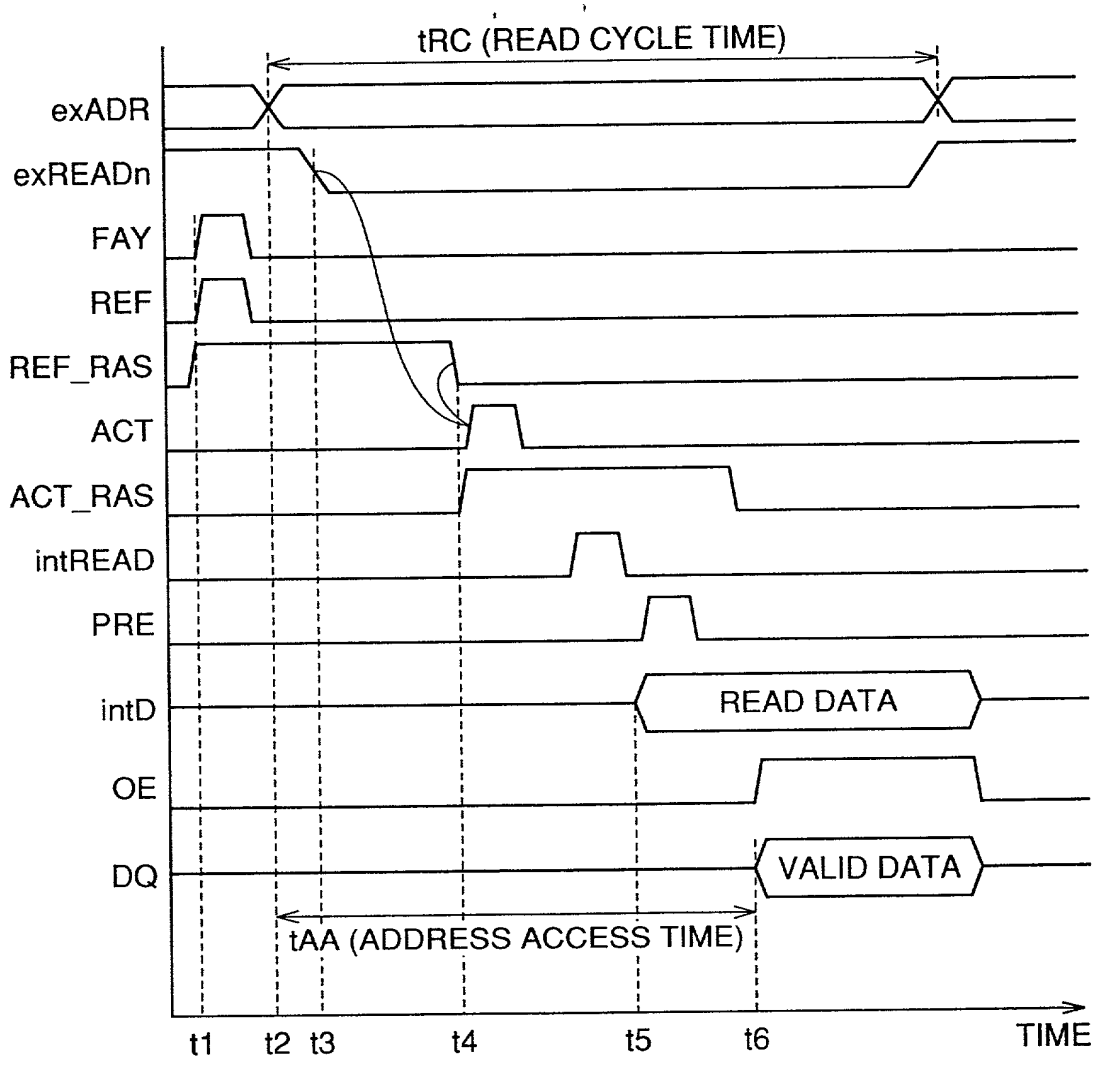
tRC (READ CYCLE TIME)
exADR
exREADn
FAY
REF
REF_RAS
ACT
ACT_RAS
intREAD
PRE
intD
READ DATA
OE
DQ
VALID DATA
tAA (ADDRESS ACCESS TIME)
t1
t2
t3
t4
t5
t6
TIME

FIG. 14

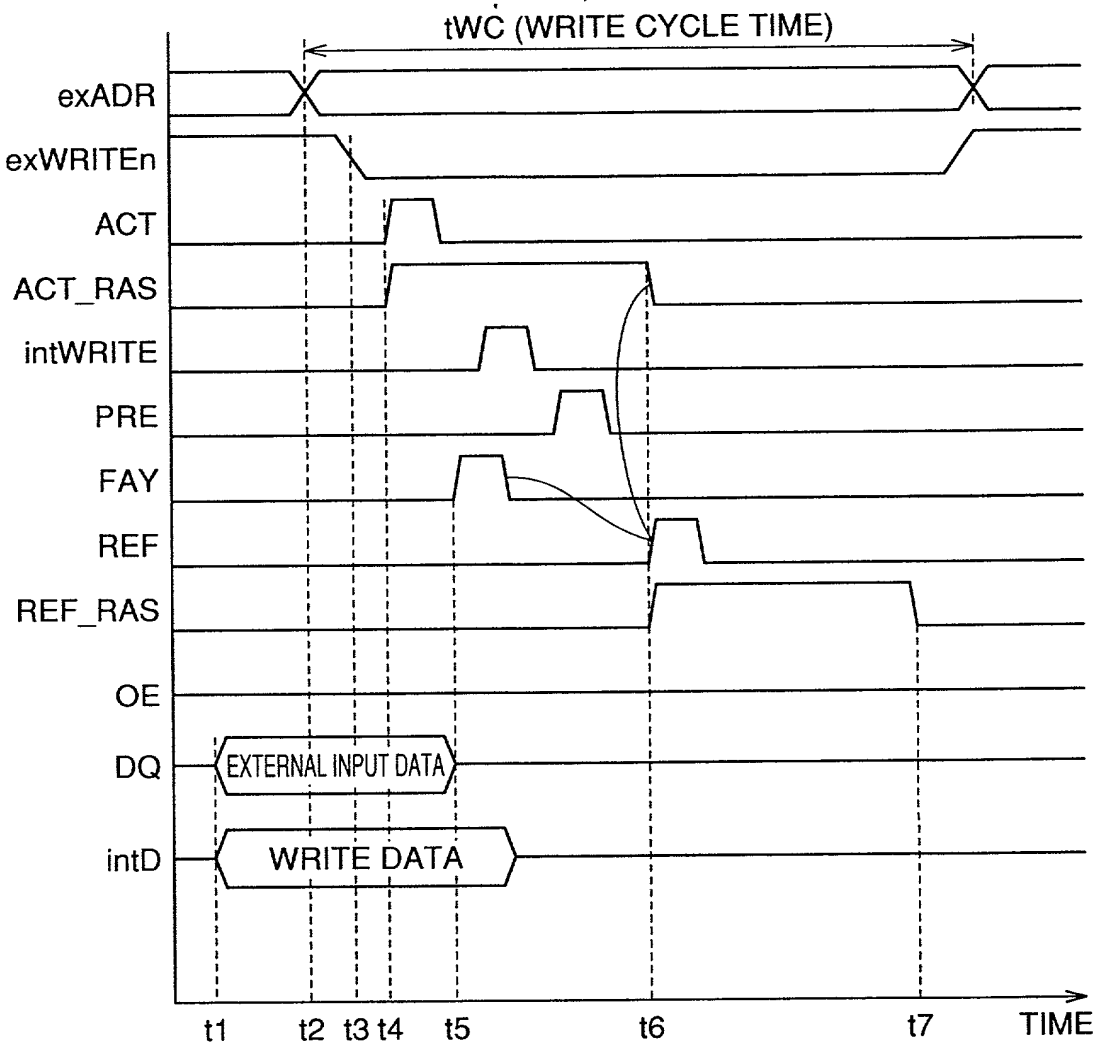
tWC (WRITE CYCLE TIME)
exADR
exWRITEn
ACT
ACT_RAS
intWRITE
PRE
FAY
REF
REF_RAS
OE
DQ
EXTERNAL INPUT DATA
intD
WRITE DATA
t1
t2
t3
t4
t5
t6
t7
TIME

FIG.15

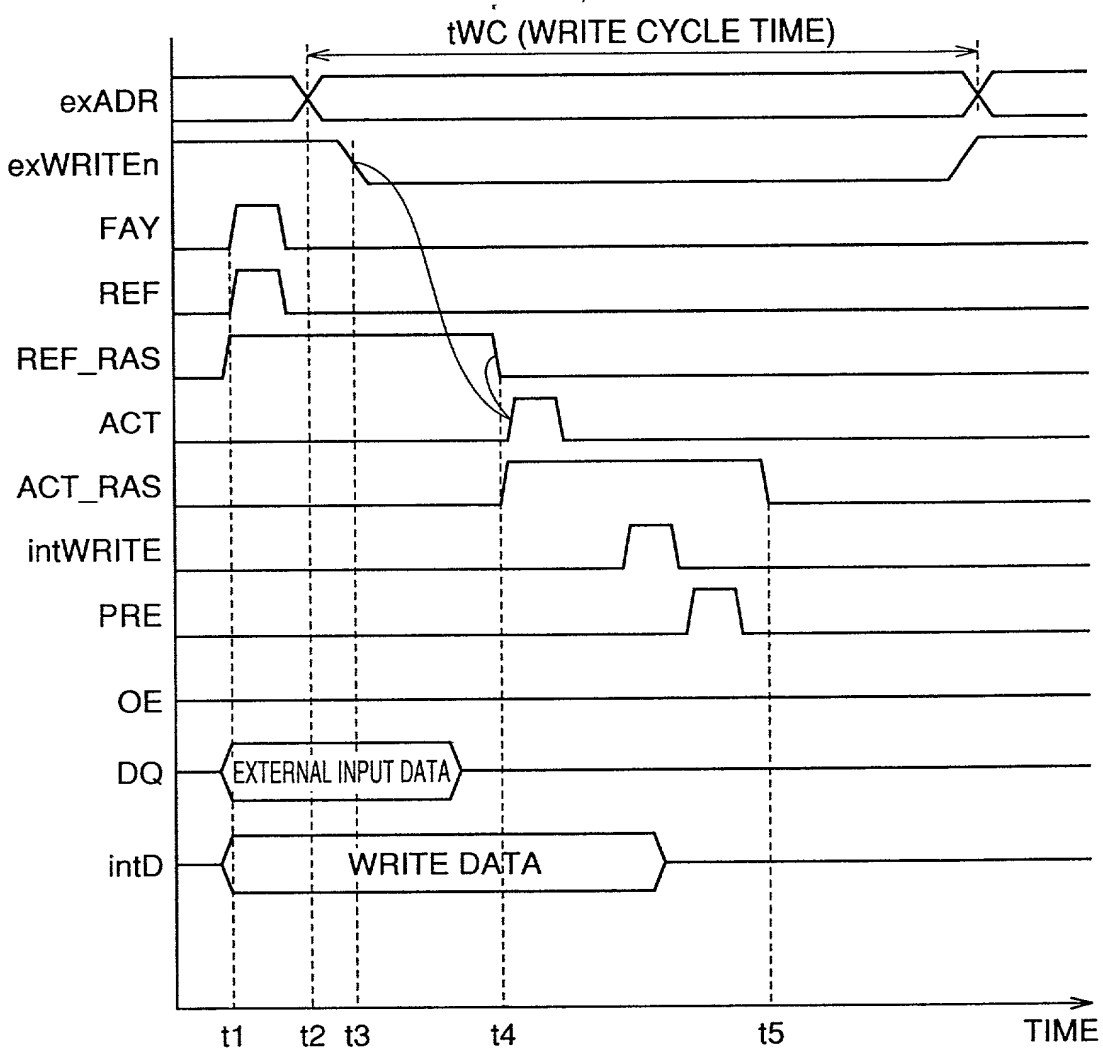
tWC (WRITE CYCLE TIME)
exADR
exWRITEn
FAY
REF
REF_RAS
ACT
ACT_RAS
intWRITE
PRE
OE
DQ
EXTERNAL INPUT DATA
intD
WRITE DATA
t1
t2
t3
t4
t5
TIME

FIG.16

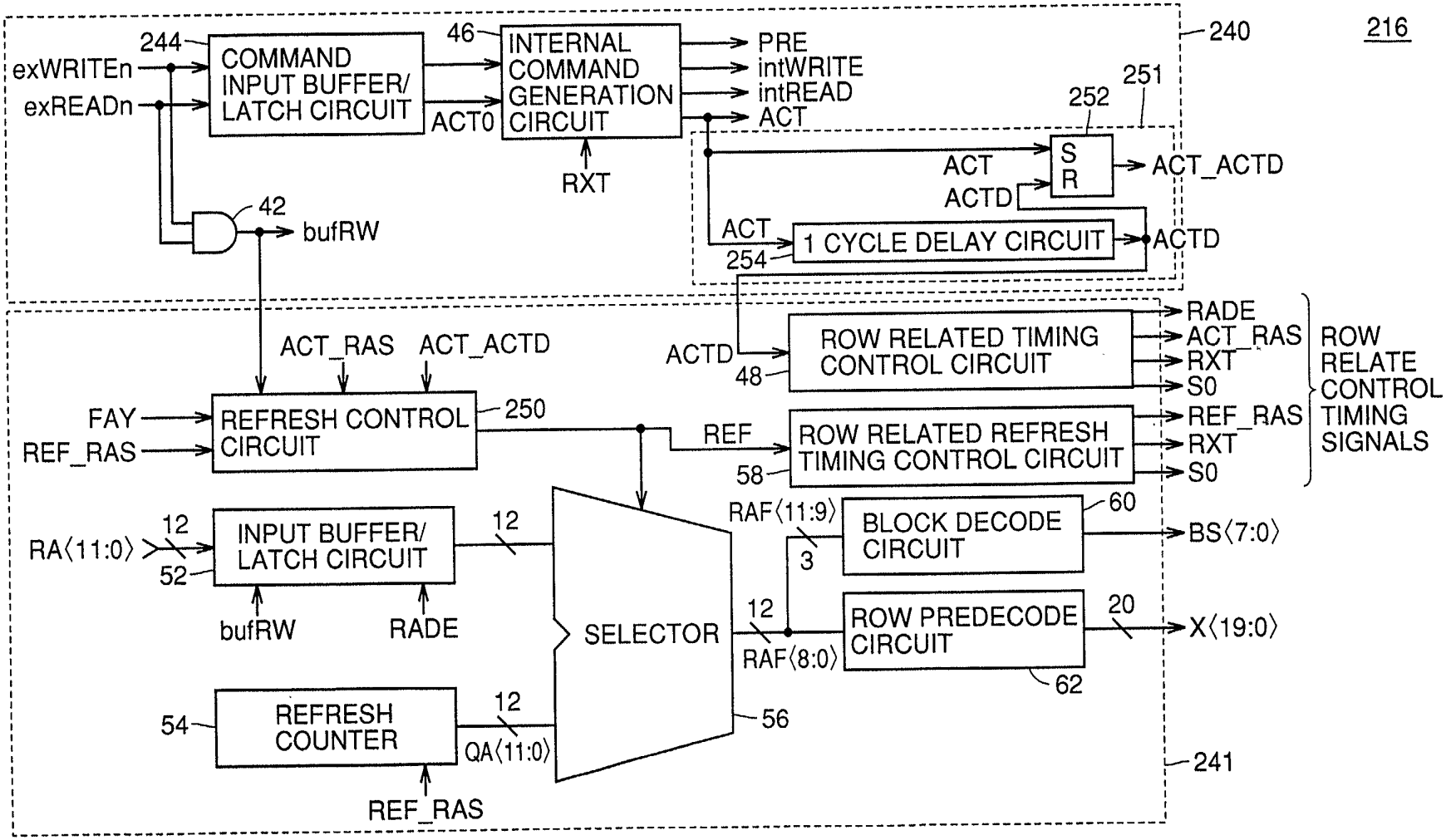
216
240
244
exWRITEn
exREADn
COMMAND INPUT BUFFER/ LATCH CIRCUIT
46
INTERNAL COMMAND GENERATION CIRCUIT
ACT0
RXT
PRE
intWRITE
intREAD
ACT
251
252
ACT
ACTD
S
R
ACT_ACTD
42
bufRW
ACT
254
1 CYCLE DELAY CIRCUIT
ACTD
ACT_RAS
ACT_ACTD
ACTD
48
ROW RELATED TIMING CONTROL CIRCUIT
RADE
ACT_RAS
RXT
S0
ROW RELATE CONTROL TIMING SIGNALS
FAY
REF_RAS
REFRESH CONTROL CIRCUIT
250
REF
58
ROW RELATED REFRESH TIMING CONTROL CIRCUIT
REF_RAS
RXT
S0
RA⟨11:0⟩
12
52
INPUT BUFFER/ LATCH CIRCUIT
12
bufRW
RADE
SELECTOR
RAF⟨11:9⟩
3
60
BLOCK DECODE CIRCUIT
BS⟨7:0⟩
12
RAF⟨8:0⟩
ROW PREDECODE CIRCUIT
20
X⟨19:0⟩
62
54
REFRESH COUNTER
12
QA⟨11:0⟩
56
REF_RAS
241

FIG.17

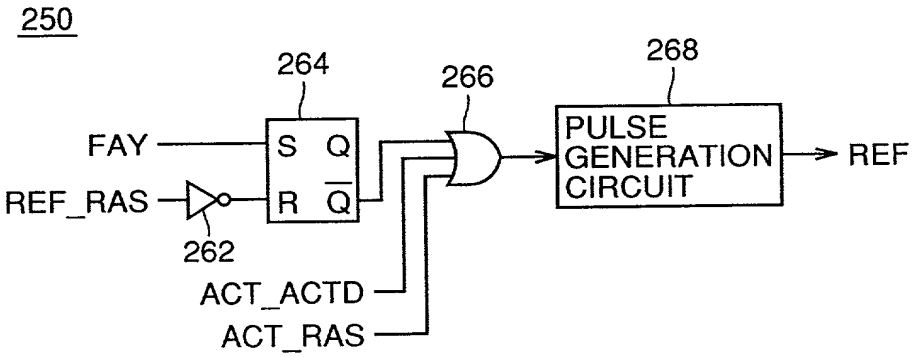
250
264
266
268
FAY
S Q
REF_RAS
R Q
262
PULSE GENERATION CIRCUIT
REF
ACT_ACTD
ACT_RAS

FIG.18

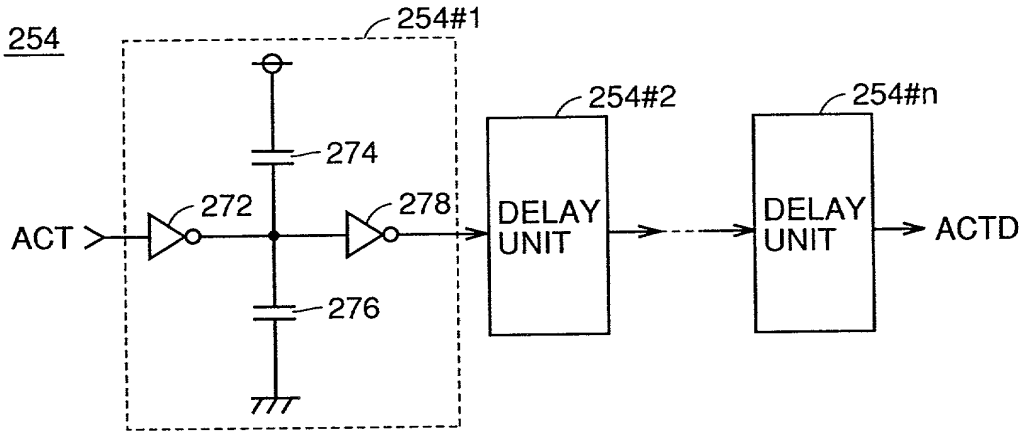
254
254#1
254#2
254#n
274
272
278
ACT
DELAY UNIT
DELAY UNIT
ACTD
276

FIG.19

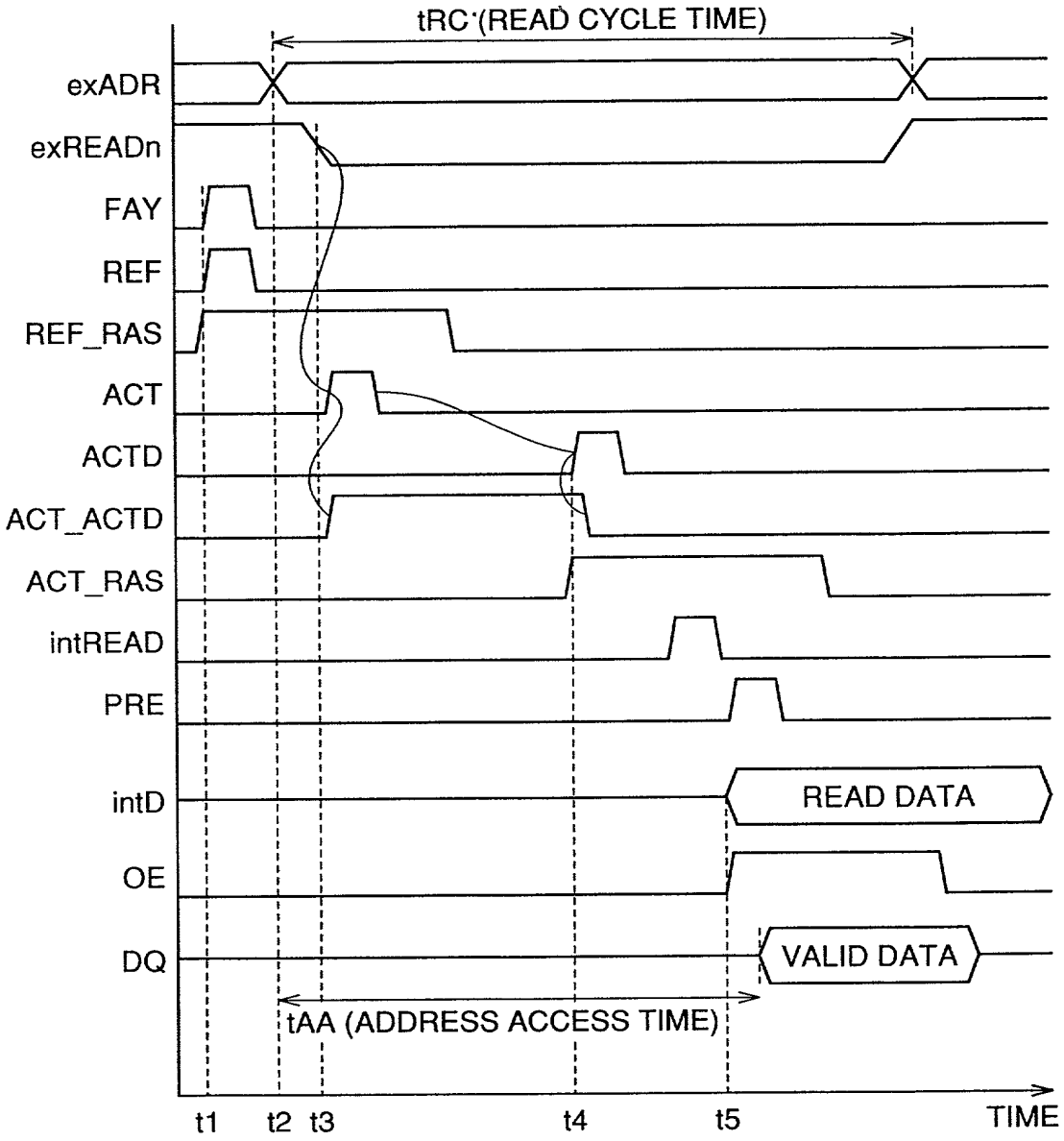
tRC (READ CYCLE TIME)
exADR
exREADn
FAY
REF
REF_RAS
ACT
ACTD
ACT_ACTD
ACT_RAS
intREAD
PRE
intD
OE
DQ
READ DATA
VALID DATA
tAA (ADDRESS ACCESS TIME)
t1
t2
t3
t4
t5
TIME

FIG.20

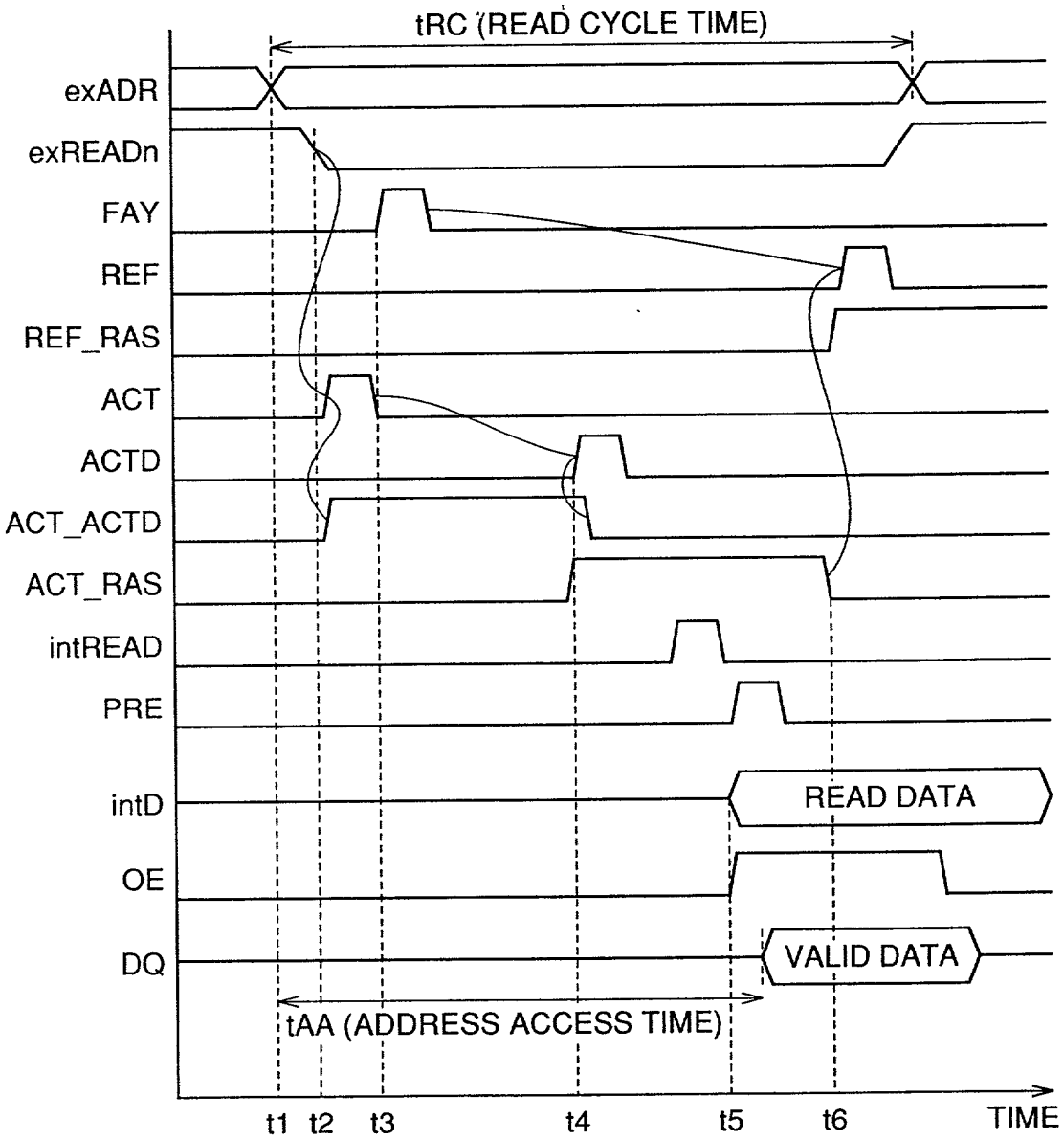
tRC (READ CYCLE TIME)
exADR
exREADn
FAY
REF
REF_RAS
ACT
ACTD
ACT_ACTD
ACT_RAS
intREAD
PRE
intD
READ DATA
OE
DQ
VALID DATA
tAA (ADDRESS ACCESS TIME)
t1
t2
t3
t4
t5
t6
TIME

FIG.21

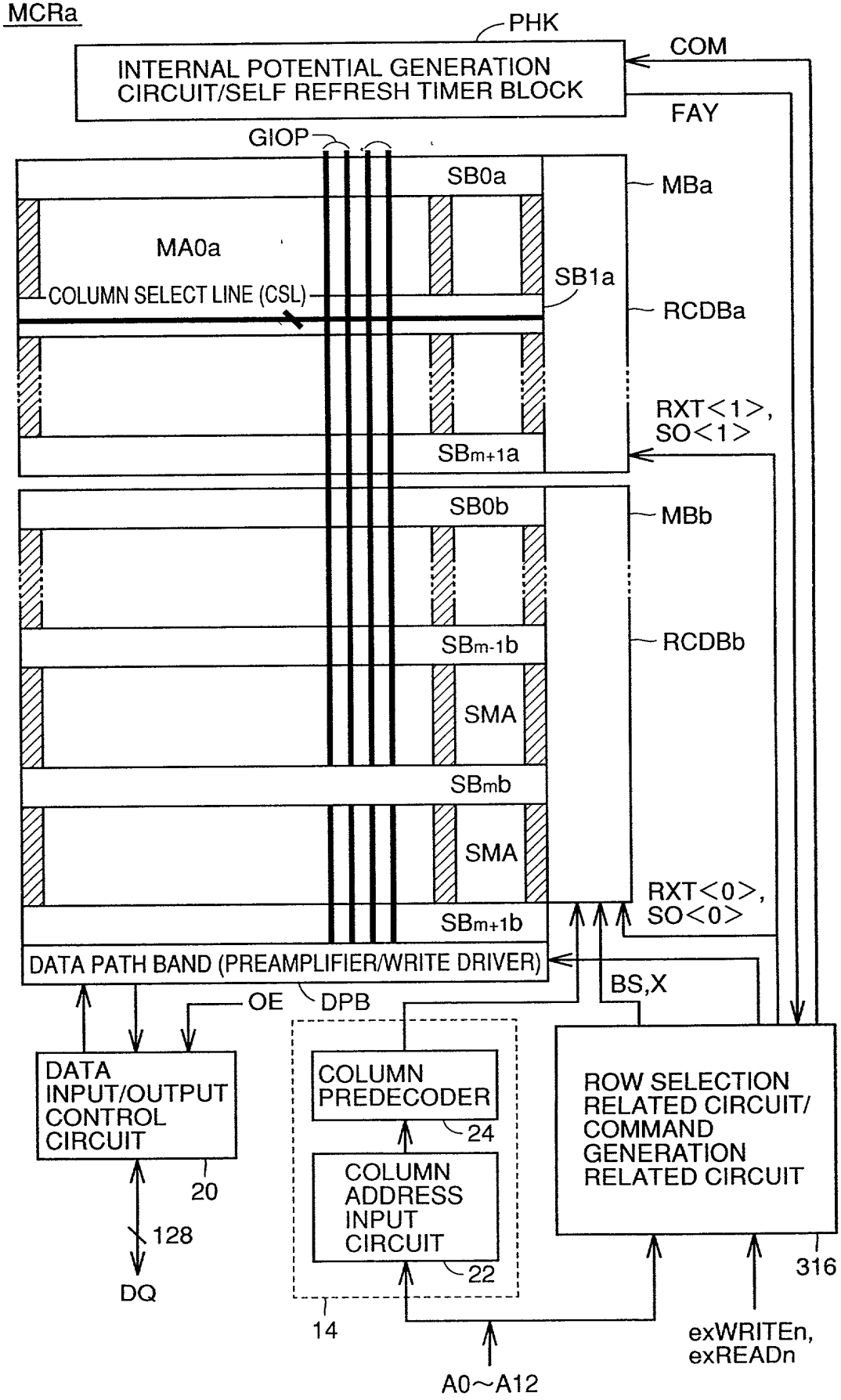
MCRa
PHK
INTERNAL POTENTIAL GENERATION CIRCUIT/SELF REFRESH TIMER BLOCK
COM
FAY
GIOP
SB0a
MBa
MA0a
SB1a
COLUMN SELECT LINE (CSL)
RCDBa
RXT<1>, SO<1>
SBm+1a
SB0b
MBb
SBm-1b
RCDBb
SMA
SBmb
SMA
RXT<0>, SO<0>
SBm+1b
DATA PATH BAND (PREAMPLIFIER/WRITE DRIVER)
BS,X
OE
DPB
DATA INPUT/OUTPUT CONTROL CIRCUIT
20
128
DQ
COLUMN PREDECODER
24
COLUMN ADDRESS INPUT CIRCUIT
22
14
ROW SELECTION RELATED CIRCUIT/ COMMAND GENERATION RELATED CIRCUIT
316
exWRITEn, exREADn
A0~A12

FIG.22

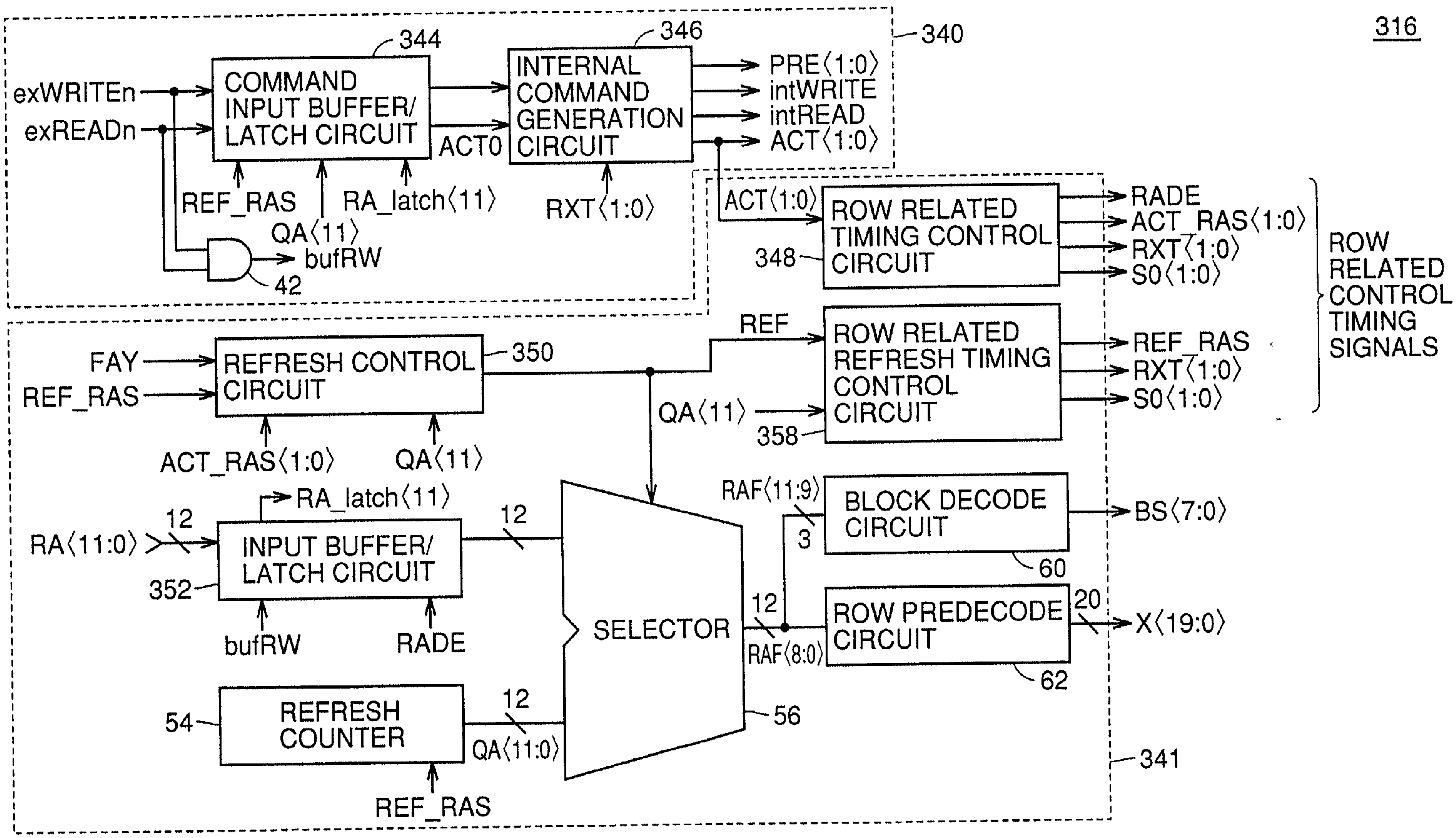
316
340
341
exWRITEn
exREADn
COMMAND INPUT BUFFER/ LATCH CIRCUIT
344
REF_RAS
RA_latch⟨11⟩
QA⟨11⟩
bufRW
42
ACT0
INTERNAL COMMAND GENERATION CIRCUIT
346
RXT⟨1:0⟩
PRE⟨1:0⟩
intWRITE
intREAD
ACT⟨1:0⟩
ACT⟨1:0⟩
ROW RELATED TIMING CONTROL CIRCUIT
348
RADE
ACT_RAS⟨1:0⟩
RXT⟨1:0⟩
S0⟨1:0⟩
ROW RELATED CONTROL TIMING SIGNALS
FAY
REF_RAS
REFRESH CONTROL CIRCUIT
350
ACT_RAS⟨1:0⟩
QA⟨11⟩
REF
QA⟨11⟩
ROW RELATED REFRESH TIMING CONTROL CIRCUIT
358
REF_RAS
RXT⟨1:0⟩
S0⟨1:0⟩
RA⟨11:0⟩
12
RA_latch⟨11⟩
INPUT BUFFER/ LATCH CIRCUIT
352
bufRW
RADE
12
SELECTOR
56
RAF⟨11:9⟩
3
BLOCK DECODE CIRCUIT
60
BS⟨7:0⟩
12
RAF⟨8:0⟩
ROW PREDECODE CIRCUIT
62
20
X⟨19:0⟩
REFRESH COUNTER
54
12
QA⟨11:0⟩
REF_RAS

FIG.23

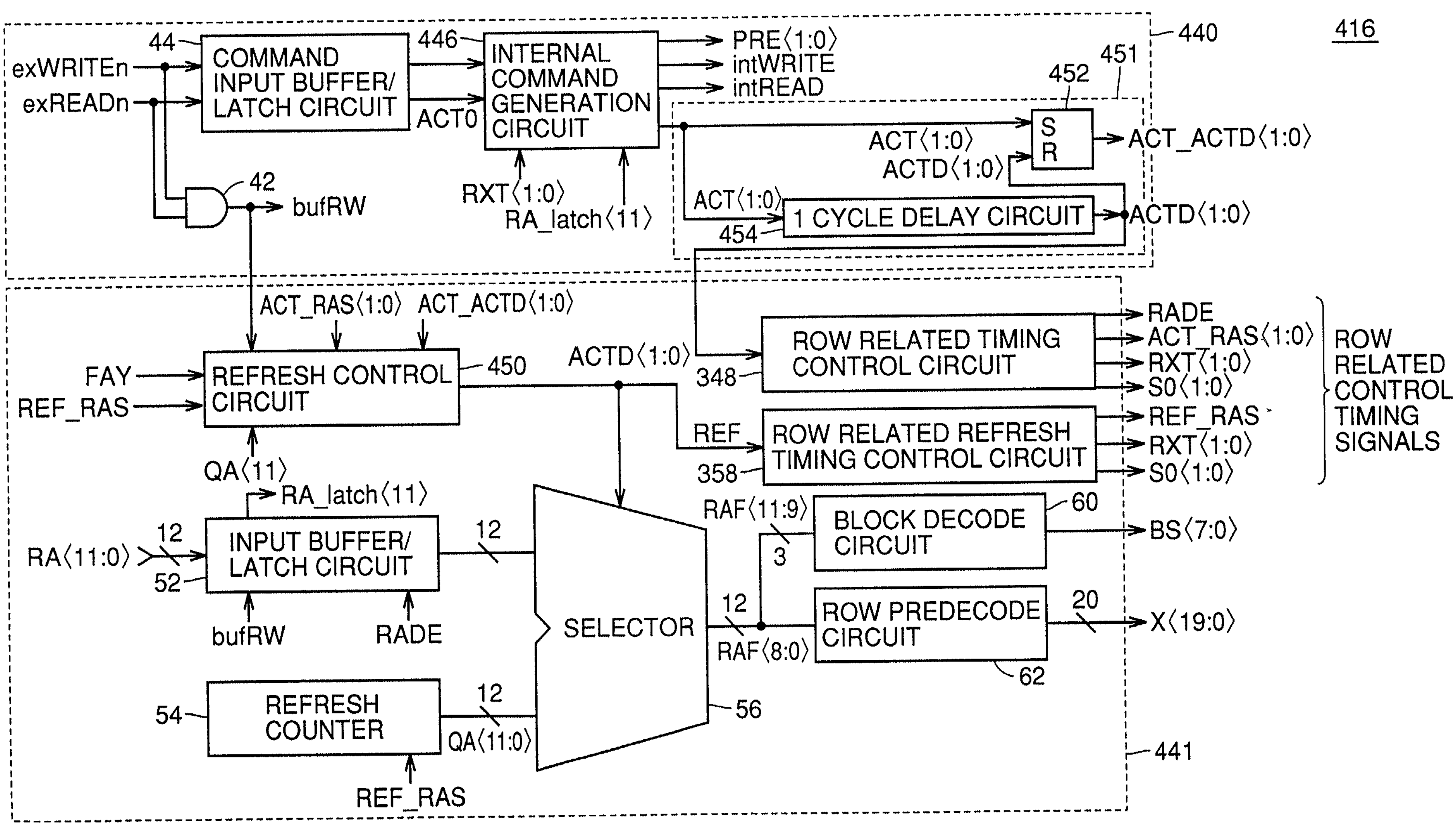
416
440
exWRITEn
exREADn
44
COMMAND INPUT BUFFER/ LATCH CIRCUIT
446
INTERNAL COMMAND GENERATION CIRCUIT
ACT0
PRE⟨1:0⟩
intWRITE
intREAD
42
bufRW
RXT⟨1:0⟩
RA_latch⟨11⟩
451
452
S
R
ACT⟨1:0⟩
ACTD⟨1:0⟩
ACT_ACTD⟨1:0⟩
ACT⟨1:0⟩
1 CYCLE DELAY CIRCUIT
454
ACTD⟨1:0⟩
ACT_RAS⟨1:0⟩
ACT_ACTD⟨1:0⟩
FAY
REF_RAS
REFRESH CONTROL CIRCUIT
450
ACTD⟨1:0⟩
348
ROW RELATED TIMING CONTROL CIRCUIT
REF
358
ROW RELATED REFRESH TIMING CONTROL CIRCUIT
RADE
ACT_RAS⟨1:0⟩
RXT⟨1:0⟩
S0⟨1:0⟩
REF_RAS
RXT⟨1:0⟩
S0⟨1:0⟩
ROW RELATED CONTROL TIMING SIGNALS
QA⟨11⟩
RA_latch⟨11⟩
RA⟨11:0⟩
12
52
INPUT BUFFER/ LATCH CIRCUIT
bufRW
RADE
12
SELECTOR
56
RAF⟨11:9⟩
3
BLOCK DECODE CIRCUIT
60
BS⟨7:0⟩
12
RAF⟨8:0⟩
ROW PREDECODE CIRCUIT
62
20
X⟨19:0⟩
54
REFRESH COUNTER
12
QA⟨11:0⟩
REF_RAS
441

FIG.24

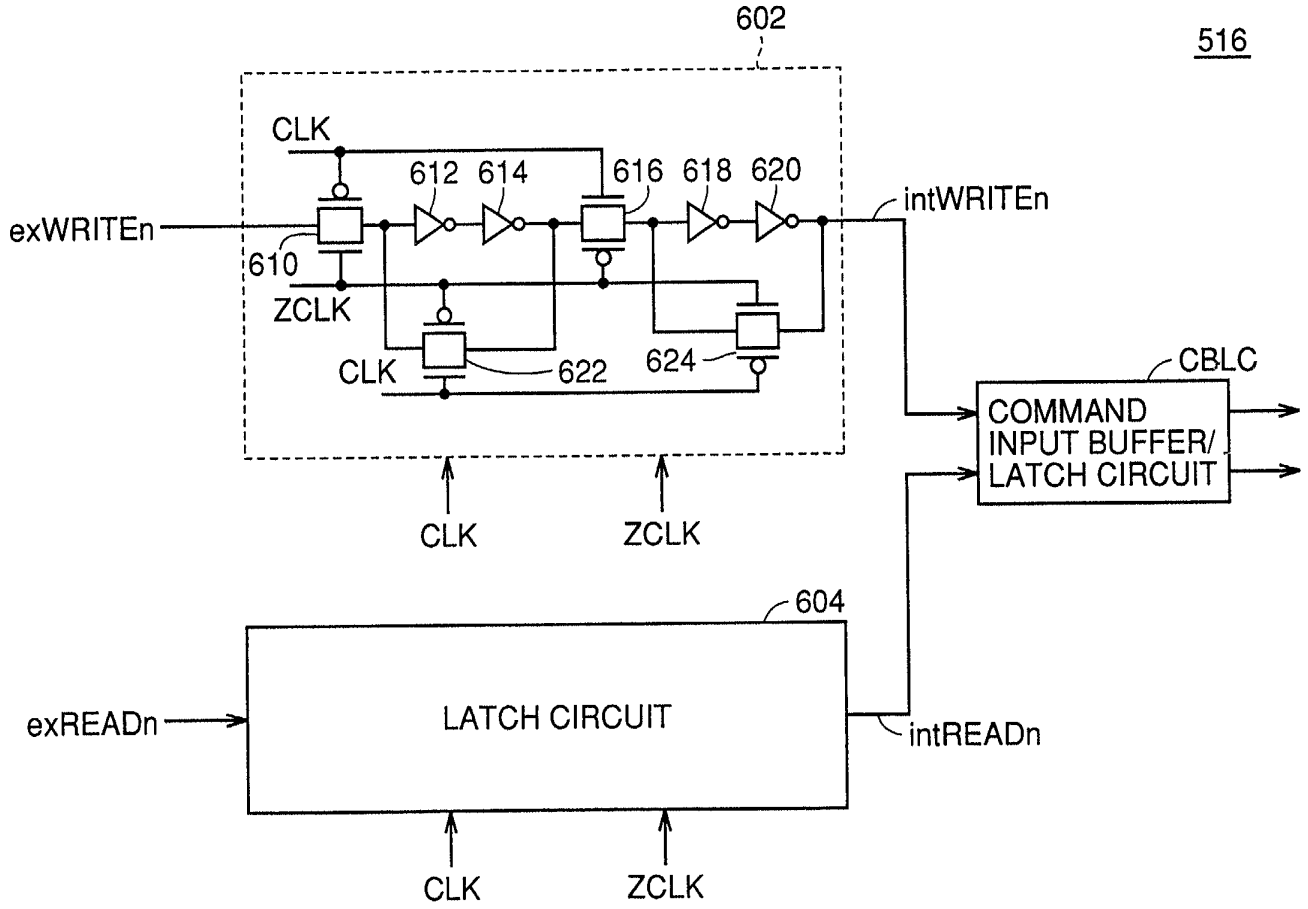
602
516
CLK
612
614
616
618
620
exWRITEn
intWRITEn
610
ZCLK
CLK
622
624
CBLC
COMMAND
INPUT BUFFER/
LATCH CIRCUIT
CLK
ZCLK
604
exREADn
LATCH CIRCUIT
intREADn
CLK
ZCLK

FIG.25

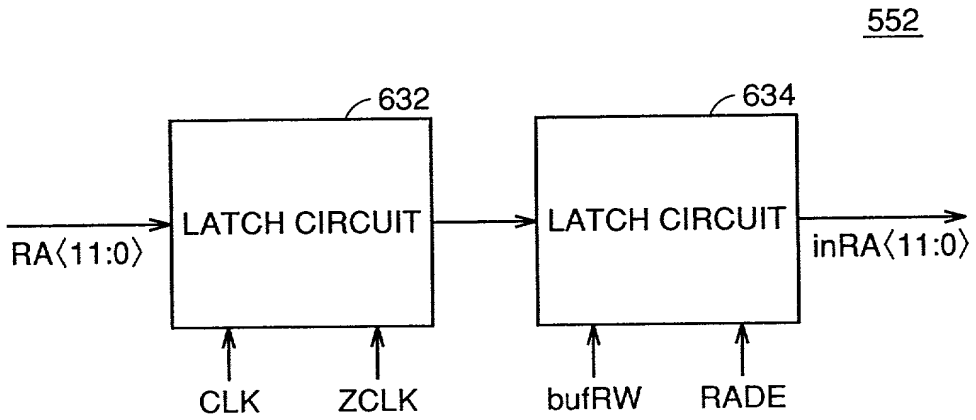
552
632
634
LATCH CIRCUIT
LATCH CIRCUIT
RA⟨11:0⟩
inRA⟨11:0⟩
CLK
ZCLK
bufRW
RADE

FIG.26

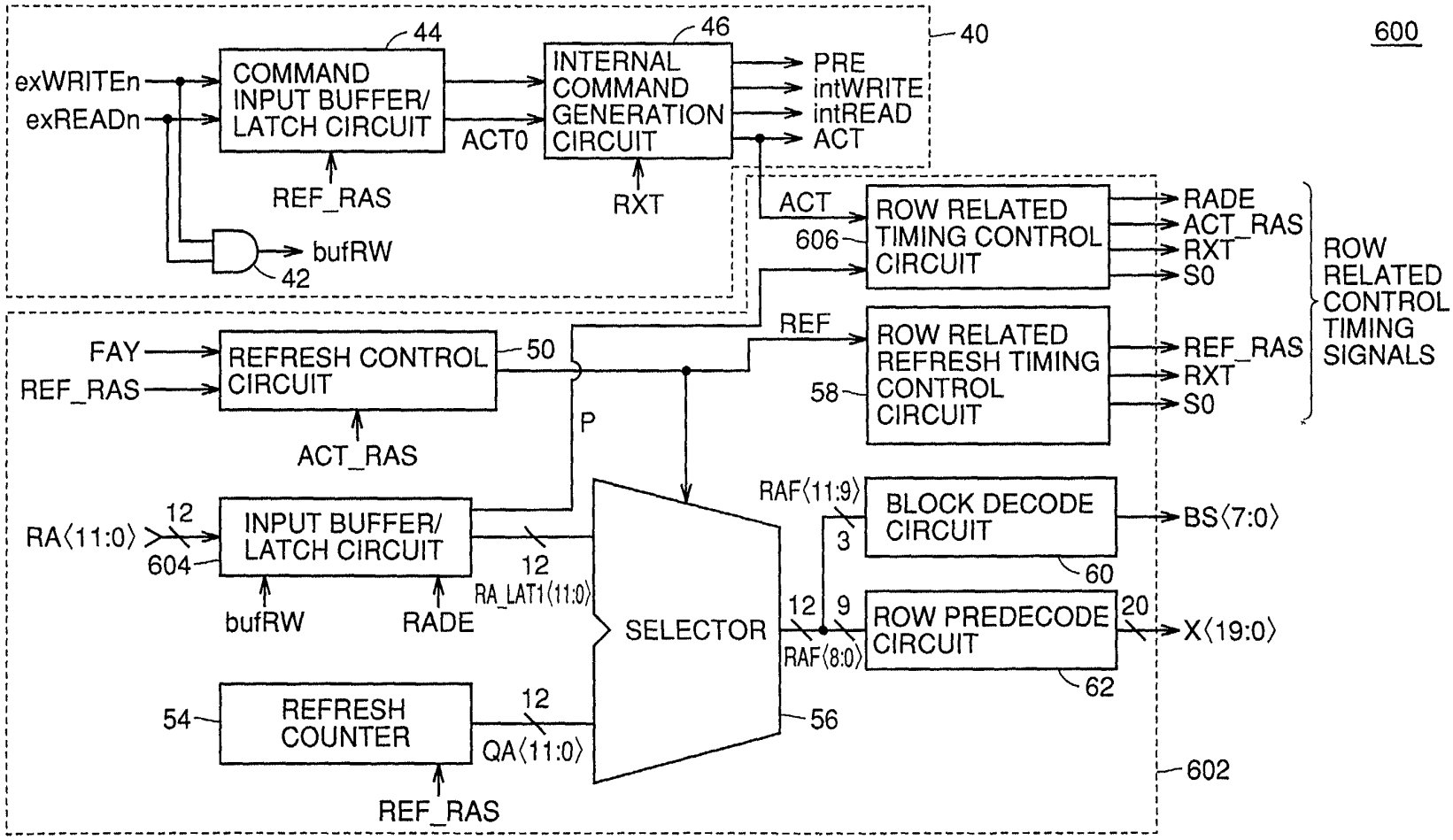

FIG.27

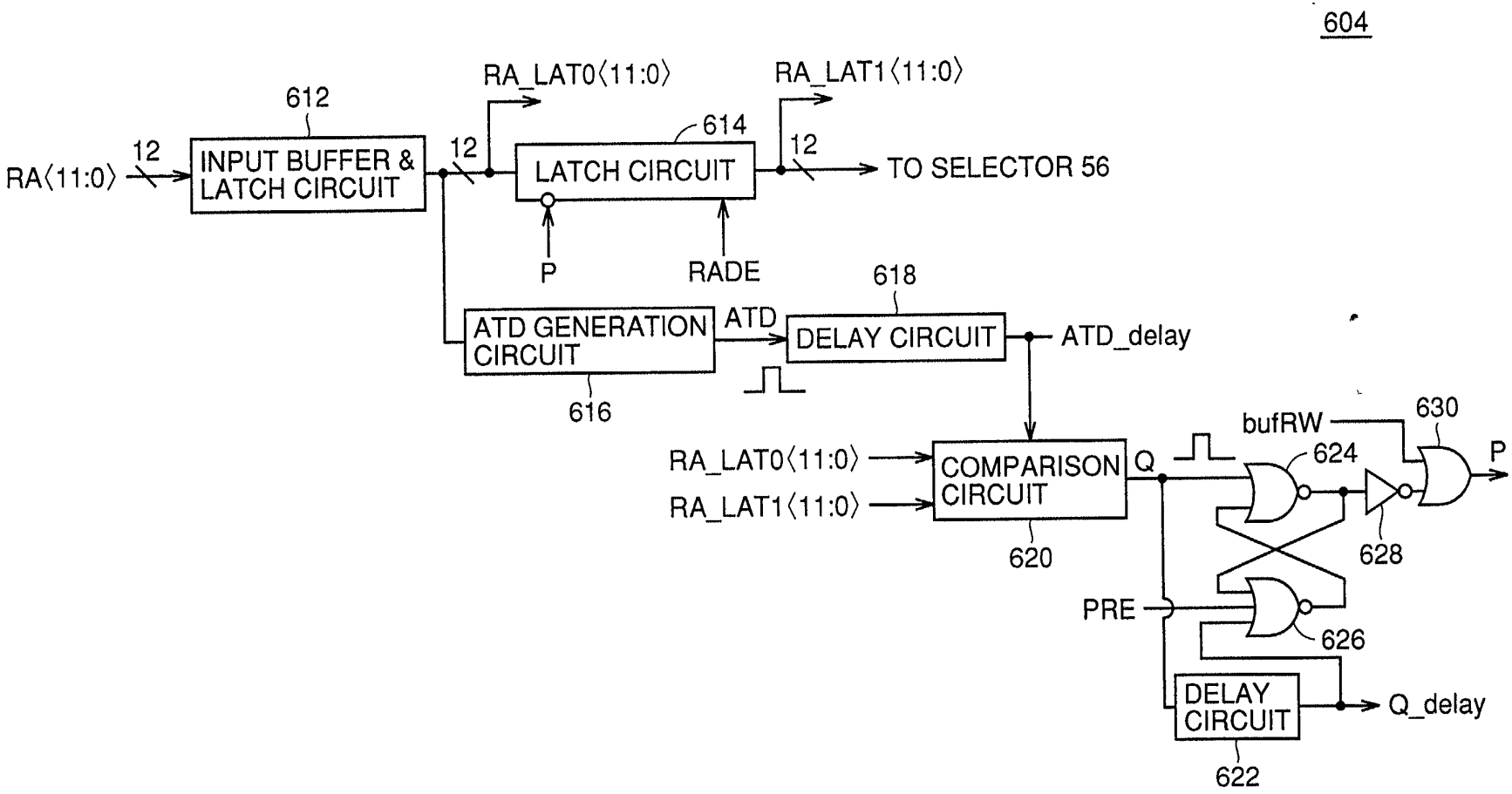
604
612
RA_LAT0⟨11:0⟩
RA_LAT1⟨11:0⟩
614
RA⟨11:0⟩
12
INPUT BUFFER & LATCH CIRCUIT
12
LATCH CIRCUIT
12
TO SELECTOR 56
P
RADE
618
ATD GENERATION CIRCUIT
ATD
DELAY CIRCUIT
ATD_delay
616
bufRW
630
RA_LAT0⟨11:0⟩
RA_LAT1⟨11:0⟩
COMPARISON CIRCUIT
Q
624
P
620
628
PRE
626
DELAY CIRCUIT
Q_delay
622

FIG.28

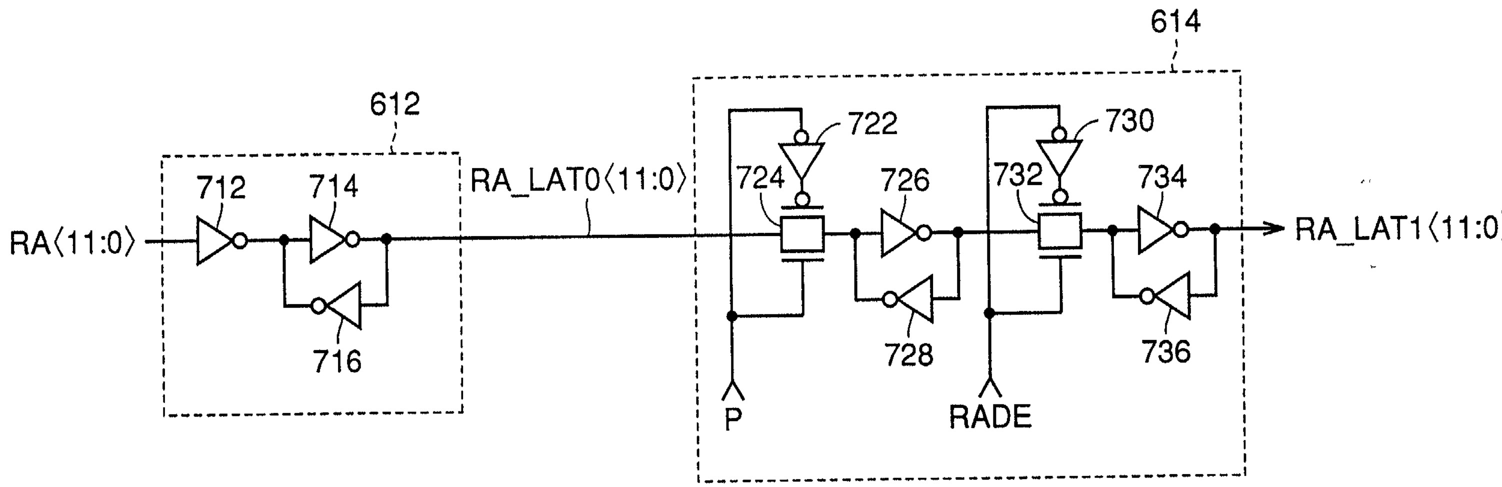
612
614
RA⟨11:0⟩
712
714
716
RA_LAT0⟨11:0⟩
722
724
726
728
P
730
732
734
736
RADE
RA_LAT1⟨11:0⟩

FIG.29

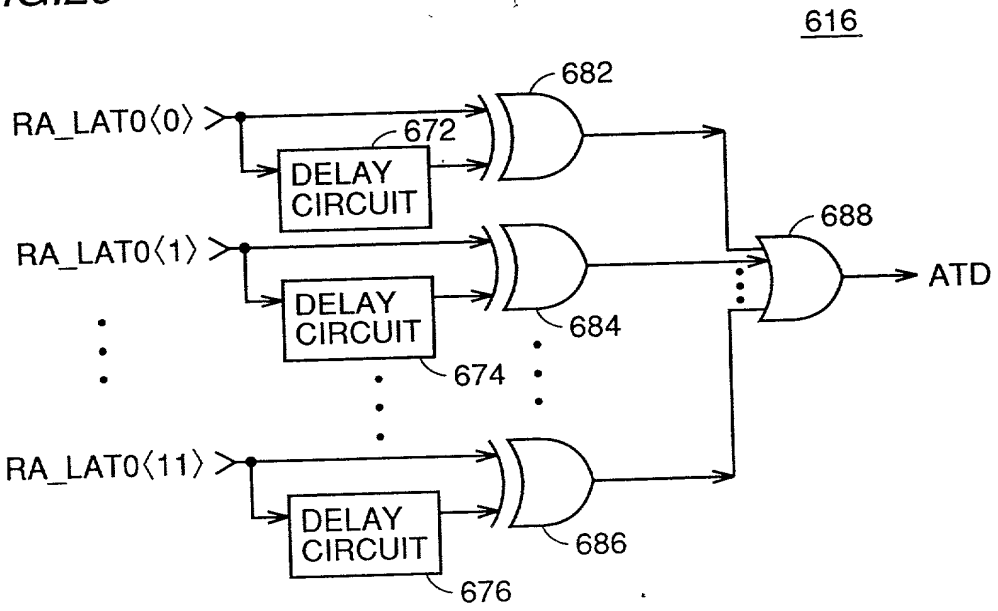
616
682
RA_LAT0⟨0⟩
672
DELAY CIRCUIT
688
RA_LAT0⟨1⟩
DELAY CIRCUIT
ATD
684
674
RA_LAT0⟨11⟩
DELAY CIRCUIT
686
676

FIG.30

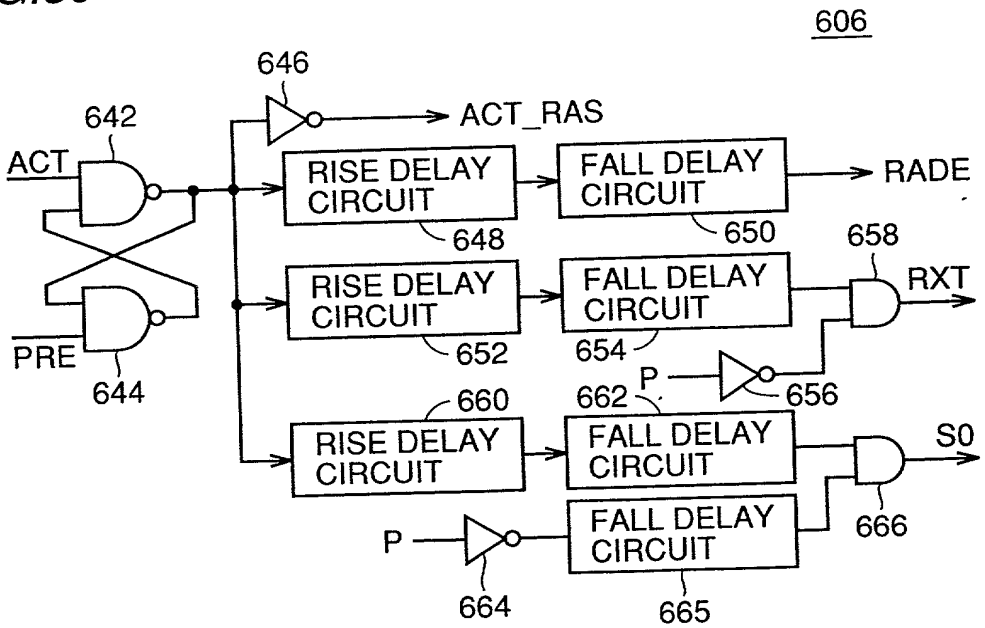
606
646
642
ACT_RAS
ACT
RISE DELAY CIRCUIT
FALL DELAY CIRCUIT
RADE
648
650
658
RISE DELAY CIRCUIT
FALL DELAY CIRCUIT
RXT
PRE
652
654
644
P
656
660
662
RISE DELAY CIRCUIT
FALL DELAY CIRCUIT
S0
FALL DELAY CIRCUIT
666
P
664
665

FIG.31

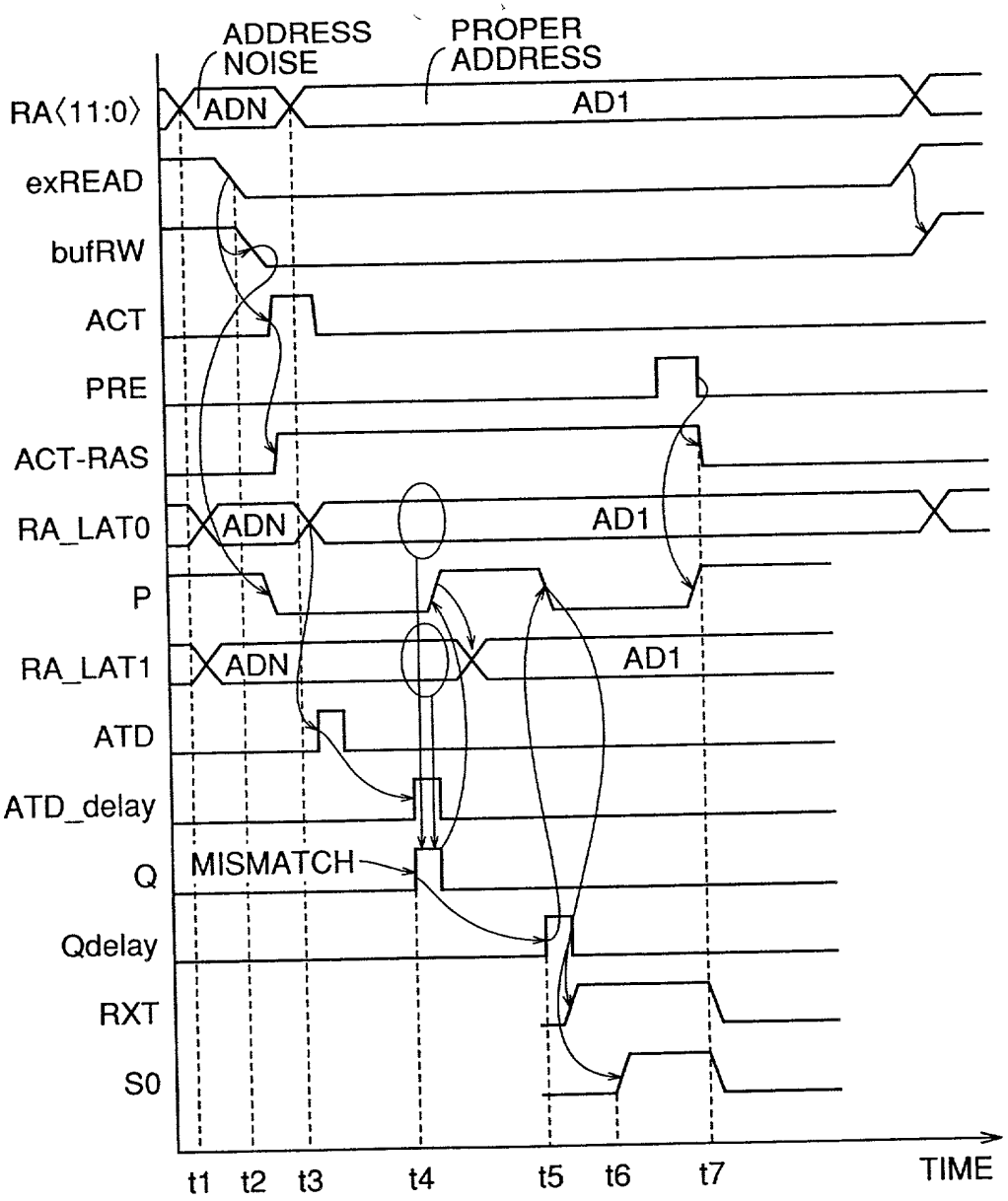
ADDRESS NOISE
PROPER ADDRESS
RA〈11:0〉
ADN
AD1
exREAD
bufRW
ACT
PRE
ACT-RAS
RA_LAT0
ADN
AD1
P
RA_LAT1
ADN
AD1
ATD
ATD_delay
Q
MISMATCH
Qdelay
RXT
S0
t1
t2
t3
t4
t5
t6
t7
TIME

FIG.32

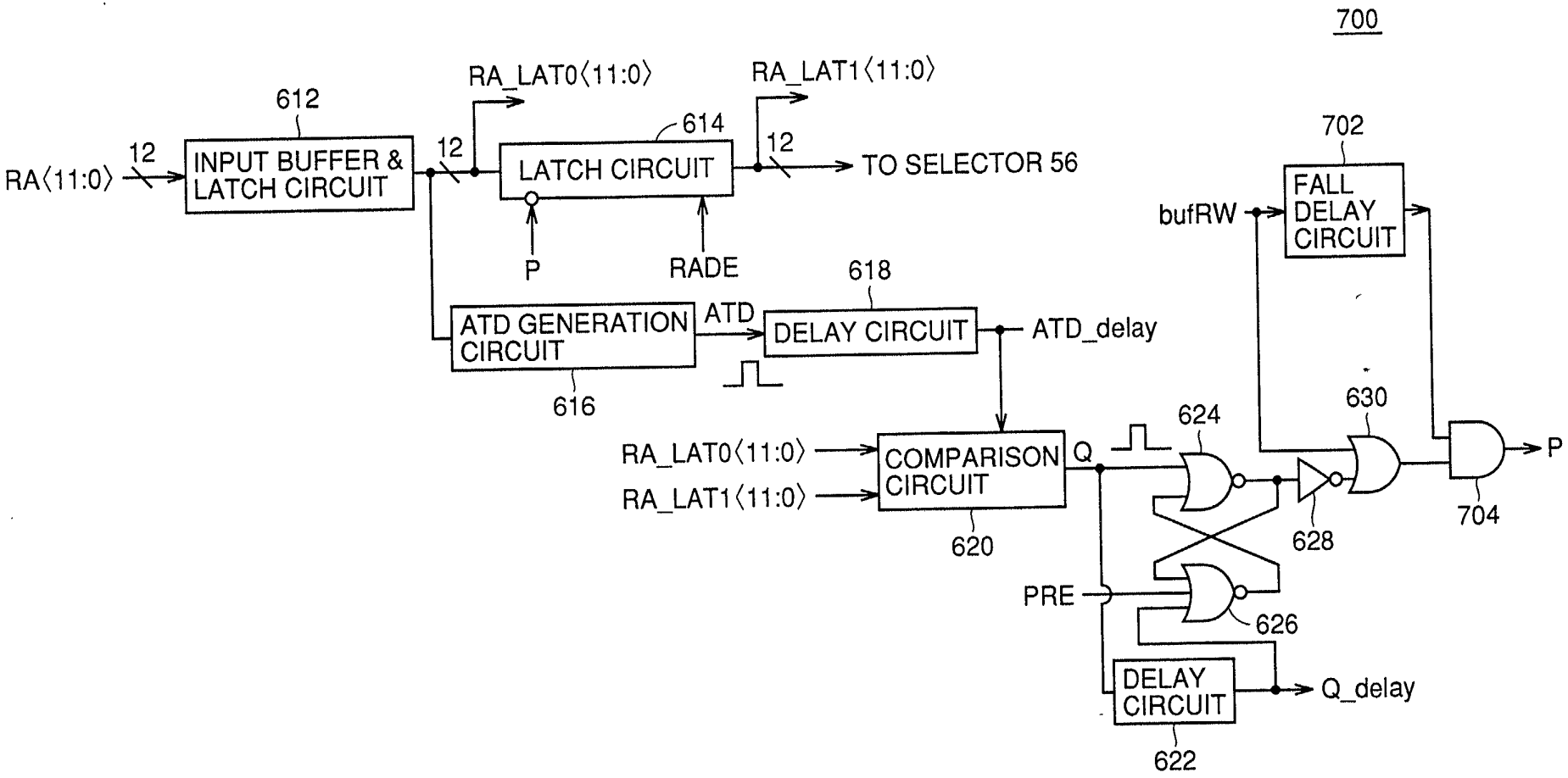
700
612
RA_LAT0⟨11:0⟩
RA_LAT1⟨11:0⟩
614
702
RA⟨11:0⟩
12
INPUT BUFFER & LATCH CIRCUIT
12
LATCH CIRCUIT
12
TO SELECTOR 56
bufRW
FALL DELAY CIRCUIT
P
RADE
618
ATD GENERATION CIRCUIT
ATD
DELAY CIRCUIT
ATD_delay
616
630
624
RA_LAT0⟨11:0⟩
RA_LAT1⟨11:0⟩
COMPARISON CIRCUIT
Q
P
704
620
628
PRE
626
DELAY CIRCUIT
Q_delay
622

FIG.33

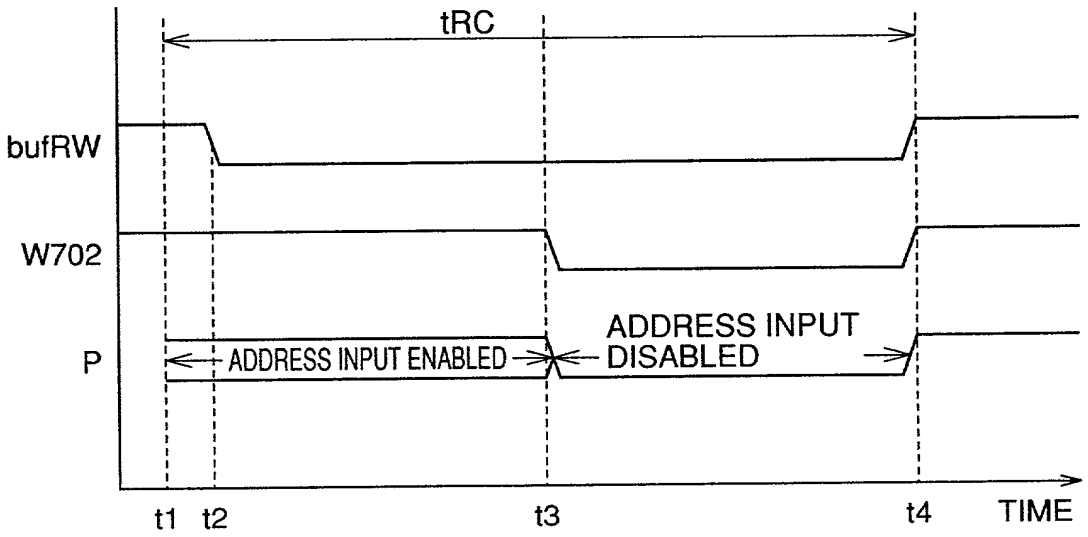
tRC
bufRW
W702
P
ADDRESS INPUT ENABLED
ADDRESS INPUT DISABLED
t1
t2
t3
t4
TIME

FIG.34 PRIOR ART